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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,187	09/24/2003	Hirotaka Nishizawa	XA-9931	4113

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1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
CARPIO, IVAN HERNAN	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/668,187	NISHIZAWA ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9-24-03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9-24-03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1,2,10,11,12 rejected under 35 U.S.C. 102(b) as being anticipated by Takiar (US Patent 5530622).

With respect to claim 1 Takiar teaches an IC card (Fig.4 and Fig. 5) comprising: a wiring substrate (Fig. 4, element 420) having an external connecting terminal (Fig. 4, element 314) and wiring; a semiconductor chip (Fig.4, element 430) disposed over the wiring substrate and connected electrically to the external connecting terminal through the wiring; and a case (Fig. 5, element 500 and 306) which covers the wiring substrate and the semiconductor chip in such a manner that the external connecting terminal of the wiring substrate is exposed, wherein the case has a first end side (Fig. 4, the right side) near which the external connecting terminal is disposed and a second end side (Fig. 4, the left side) positioned on an opposite side to the first end side, and wherein a planar outline of the wiring substrate is smaller than half of a planar outline of the case, and the wiring substrate is disposed in an area of the case closer to the first end side with respect to a middle position between the first and the second end side.

With respect to claim 2 and with all the limitations of claim 1, Takiar teaches that the semiconductor chip is disposed in an area of the case closer to the first end (fig. 4,

note element 430 is closer to the right side) side with respect to the middle position between the first and the second end side.

With respect to claim 10 Takiar teaches an IC card (Fig.4 and Fig. 5) comprising: a wiring substrate (Fig. 4, element 420) having an external connecting terminal (Fig. 4, element 314) and wiring; a semiconductor chip (Fig.4, element 430) disposed over the wiring substrate and connected electrically to the external connecting terminal through the wiring; and a case (Fig. 5, element 500 and 306) which covers the wiring substrate and the semiconductor chip in such a manner that the external connecting terminal of the wiring substrate is exposed, wherein a planar outline of the wiring substrate is smaller than half of a planar outline of the case, and wherein the case comprises: a first end side (Fig. 4, the right side) near which the external connecting terminal is disposed; a second end side (Fig. 4, the left side) positioned on an opposite side to the first end side; a first area (Fig. 4, the area where element 420 is) closer to the first end side with respect to a middle position between the first and the second end side, with the wiring substrate being disposed in the first area; and an insulating, second area (Fig. 5, the space between element 408 and the bottom cover 306) positioned between the first area and the second end side.

With respect to claim 11 Takiar teaches an IC card (Fig. 4 and Fig. 5) comprising: a wiring substrate (Fig. 4, element 420) having a plurality of external connecting terminals (Fig. 4, element 314) and wiring; a semiconductor chip (Fig. 4, element 430) disposed over the wiring substrate and connected electrically to the external connecting terminals through the wiring; and a case (Fig. 5, element 500 and 306)

having an opening into which some of the plural external connecting terminals are exposed, the case covering the wiring substrate and the semiconductor chip and further covering some of the other external connecting terminals (Fig. 5, note that the case element 500 and 306 cover the external connecting terminals 314).

With respect to claim 12 and with all the limitations of claim 11, Takiar teaches that case has a first end side (Fig. 4, the right side) near which the external connecting terminal is disposed and a second end side (Fig. 4, the left side) positioned on an opposite side to the first end side, and wherein a planar outline of the wiring substrate is smaller than half of a planar outline of the case, and the wiring substrate is disposed in an area of the case closer to the first end side with respect to a middle position between the first and the second end side.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar in view of Feldman (US Patent 5846092).

With respect to claim 3 and with all the limitations of claim 1, Takiar teaches a first and second case. Takiar does not teach one that of the first and the second case

having a projecting portion in an area other than the area where the wiring substrate is disposed, the other case having a recess portion in an area other than the area where the wiring substrate is disposed, the projecting portion being fitted in the recess portion so as to connect the first and the second case with each other. Feldman teaches an IC card with a first case (Fig. 4a, element 44) and a second case (Fig. 4a, element 42) and that the first case has projecting portion (Fig. 5, element 94) in an area other than where the wiring substrate is disposed and the second case has a recess portion (Fig. 5, element 92 the recess formed by vertical projection and angled projection) in an area other than where the wiring substrate is disposed, and that the projecting portion is fitted in the recess so as to connect he first and the second case with each other. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the projection and recess connecting mechanism taught by Feldman to connect the two cases of the IC card taught by Takiar because with this connecting mechanism no tools are need to connect the two cases.

With respect to claim 4 and with all the limitations of claim 3, Feldman teaches a tip-side inner periphery portion of the recess portion and a tip-side outer periphery portion of the projecting portion are chamfered.

With respect to claim 5 and with all the limitations of claim 3, Feldman teaches that the recess portion and the projecting portion have an aligning function (Fig. 4a; Note that do to the projection portion and the recess portion the cases will only connect if the projection portion is placed directly over the recess portion, thus an aligning

function) for self-alignment wise aligning planar positions of the first and the second case when both said cases are superimposed one over the other.

With respect to claim 6 and with all the limitations of claim 3, Feldman teaches that the projecting portion formed over the first case has a function (Fig. 5, element 90 of the 1st case can be used to connect the case to a carrier, much in the same way it connects to the 2nd case) for fixing the case formed with the projecting portion to a carrier temporarily.

Claims 7- 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar in view of Hara (US Patent 4797542).

With respect to claim 7 and with all the limitations of claim 1, Takiar teaches a first case, a second case and a wiring substrate but does not teach a movable switch, and in the first or the second case, a mechanism for holding the movable switch is provided in an area other than the area where the wiring substrate is disposed. Hara teaches a movable switch (Fig. 5, element 62), wherein the case comprises a first case (Fig. 5, element 11) and a second case (Fig. 5, element 10), and in the first or the second case, a mechanism (Fig.l 5, element 63) for holding the movable switch is provided in an area other than the area where the wiring substrate (Fig. 5, element 20) is disposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch taught by Hara with the IC card taught by Takiar for the purpose of turning on and off the IC Card (Hara column 7, lines 8-48).

With respect to claim 8 and with all the limitations of claim 1, Takiar teaches a first case, a second case and a wiring substrate but does not teach a movable switch, and a click mechanism for the movable switch is provided in an area other than the area where the wiring substrate is disposed. Hara teaches a movable switch (Fig. 5, element 62) and a click mechanism (column 7, lines 44-48) for the movable switch is provided in an area other than the area where the wiring substrate is disposed.

With respect to claim 9 and with all the limitations of claim 1, Takiar teaches that the case comprises a first case (fig. 5, element 500) and a second case (Fig. 5, element 306) and a means (Fig, 5, element 200, note the projection on the left part of the case can be inserted into a recess of appropriate size on a carrier thus fixing the case to the carrier) for fixing the first and the second case to a carrier temporarily are provided in areas of the first and the second case other than the area where the wiring substrate is disposed. Takiar does not teach a moveable switch. Hara teaches a movable switch (Fig. 5, element 62). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch taught by Hara with the IC card taught by Takiar for the purpose of turning on and off the IC Card (Hara column 7, lines 8-48).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US patent 5529503 discloses a jacketed IC Card. US Patents 5544007, 5502620 and 6295206 discloses and IC card with semiconductor device and terminals. US patent 6295206 discloses an IC card with a switch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IC

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